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D. Remarks

Rejection of Claims 49-58 Under 35 U.S.C. §102(b) based on U.S. Patent No. 5,436,481 (*Egawa et al.*).

Prior to explicitly addressing particular claim limitations, Applicant believes it would be beneficial to establish some basic transistor terminology in order to clarify the basis upon which the claims are currently rejected.

The rejection of Applicant's claims has been maintained based on the following argument:

> Egawa et al teach... that is it beneficial to introduce P-type impurities into the... gate electrode of a P-channel MOS transistor...[1]

Applicant readily concedes this teaching is present in the cited reference. However, the rejection then proceeds to define a P-channel MOS transistor in contravention to standard definitions, and in contravention to explicit definitions set forth in the cited references:

> ... a P-channel MOS transistor (in other words, the transistor has a P-type channel, N-type source and drain regions and P-type silicon as the gate electrode)...[2]

As is well established, P-channel (or P-type) transistors do not have N-type source and drain regions. N-channel (or N-type) transistors have N-type source and drain regions. Similarly, P-channel (or P-type) transistors have **P-type** source and drain regions. Transistors are defined according to "channel" types based on operation. For example, enhancement mode P-channel transistors have N-type channels, and such channels are inverted to p-type by application of a gate voltage.

In short, the following is the well established accepted terminology for transistor types:

[1] See the Final Office Action, dated 11/07/03, Page 4, Lines 16-18.
[2] See the Final Office Action, dated 11/07/03, Page 4, Lines 18-19.

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N-channel transistors: N-type source and drain

P-channel transistors: P-type source and drain.

This well established meaning is reflected in the very references raised during prosecution.

U.S. Patent No. 4,990,974 issued to *Vinal* shows a p-channel transistor has p-type sources and drains.

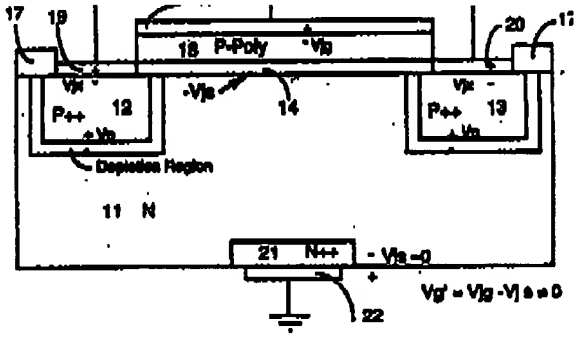
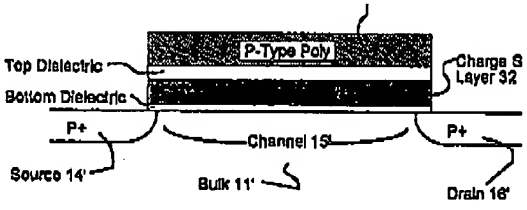


Figure 10C

"FIGS. 10C-10D illustrate P-channel devices." (*Vinal*, Col. 20, Lines 62-63).

Vinal indicates a p-channel transistor has a P-type source and drain (12 and 13). Reference to FIGS. 10A and 10B of *Vinal* also indicates that this reference shows an n-channel transistor has an N-type source and drain.

U.S. Patent No. 6,140,676 (*Lancaster '676*) issued to the present inventor is no different.



PRIOR ART
FIG. 2

"In FIG. 2 memory transistor 10' shows a P-channel non-volatile insulated gate field effect transistor..." (*Lancaster '676*, Col. 2, Lines 21-22).

That is, source 14' and drain 16' of the p-channel transistor are clearly P-type.

Egawa et al., the reference upon which all present claims are rejected, follows the same well established convention: P-channel transistors have **p-type sources and drains**.

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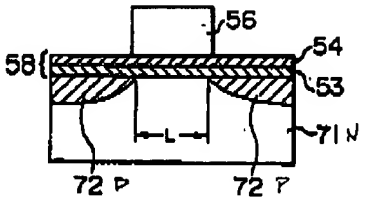
FIG. 12



"Referring to FIG. 12, description will next be made of a... device... wherein all... transistors are P-channel type... a pair of P-type diffused layers 72...formed in N-type semiconductor substrate 71..." (*Egawa et al.*, Col. 10, Lines 11-21)

The above is believed to be clear evidence that the term "P-channel MOS transistor" as used in *Egawa et al.*, and as well understood by those skilled in the art, does not mean a "transistor has a P-type channel, N-type source and drain regions and P-type silicon as the gate electrode" as argued in the rejection. In fact, the meaning is the exact opposite of what is being argued, namely that a p-channel transistor has P-type source and drain regions.

The understanding of transistor terminology having been clearly established, Applicant can only reiterate the arguments presented in the previous response to office action.

The invention of claim 49 is directed to a method for making a non-volatile semiconductor device. The method includes forming a multilayer gate dielectric having a charge storage layer. Such a charge storage layer is dielectrically equivalent to a layer of silicon dioxide having a thickness that is less than 200 angstroms. The method also includes forming a gate comprising polycrystalline silicon of a first conductivity type on said gate dielectric. The method further includes forming source and drain regions separated by a channel region in a semiconductor substrate, said source and drain regions having a second conductivity type different from said first conductivity type.

Thus, Applicant's claim 49 invention clearly recites forming a gate electrode of a first conductivity type that is different than that of the source and drain regions, which have a second conductivity type.

As is well known, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference. Because the reference *Egawa et al.* does not show all elements of claim 49, this ground of rejection is traversed.

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Egawa et al. teaches as MOS transistor having a structure basically the same as a metal-oxide-nitride-oxide-semiconductor (MONOS) or silicon-oxide-nitride-oxide-semiconductor (SONOS) type device. However, *Egawa et al.* never shows a gate electrode having different conductivity type than the corresponding source and drain regions. Each of the examples in *Egawa et al.* will be reviewed, and shown to either not show the above claim limitation, or clearly teach away from the claim limitation.

The "Background of the Invention" section of *Egawa et al.* describes a metal-oxide-semiconductor (MOS) type transistor with a polycrystalline silicon gate. However, the gate has no particular conductivity type, let alone a different conductivity type than that of source and drain regions:

> [A] polycrystalline Si film 17 is formed in a pattern of the gate electrode...[3]

The first, second, and third embodiments of *Egawa et al.* are no different than the Background of Invention example, describing no particular gate conductivity type, let alone a different conductivity type than that of source and drain regions:

> Then, as shown in FIG. 4B, a polysilicon 24 is deposited to a thickness of 300 nm by the CVD process.[4]

> [A] polycrystalline Si film 37 is formed in a pattern of a gate electrode and diffused layers 38 of source and drain are formed in the Si substrate 32 on both sides of the polycrystalline Si film 37.[5]

> [A] polysilicon layer 56 as the gate electrode is deposited on the upper silicon oxide film 55 by the low pressure CVD process (FIG. 10C).[6]

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[3] *Egawa et al.*, Col. 1, Lines 53-54, referring to FIG. 1.
[4] *Egawa et al.*, Col. 4, Lines 34-35, referencing the first embodiment.
[5] *Egawa et al.*, Col. 6, Lines 10-14, referencing the second embodiment.
[6] *Egawa et al.*, Col. 9, Lines 1-3, referencing the third embodiment.

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The fourth embodiment of *Egawa et al.* teaches away from Applicant's claim 49 limitations, by teaching a gate electrode having the same conductivity type as the source and drain regions:

> A MOS field-effect transistor of the semiconductor device comprises a pair of second conductivity type diffused layers 52 (***N-type diffused layers 62***), a gate insulating film 58, and a gate electrode 56 made of an ***N-type polysilicon***.[7]

In summary, none of the examples of *Egawa et al.* teach the formation of gate having different conductivity type than source and drain regions. Further, the fourth embodiment of *Egawa et al.* teaches away from Applicant's claim limitations by teaching the formation of a gate having the same conductivity type as a source and drain.

Thus, the reference does not show all limitations of claim 49, and this ground for rejection is traversed.

Various claims depending from claim 49 have additional claim limitations that are not shown in the cited reference.

Claim 57 recites that forming a polycrystalline silicon gate doped to an n-type conductivity, and source and drain regions having a p-type conductivity. Conversely, claim 58 recites forming a polycrystalline silicon gate doped to a p-type conductivity, and source and drain regions having an n-type conductivity.

As noted above, forming such structures to have different conductivity types is not shown in *Egawa et al.*

For all of these reasons, this ground for rejection is traversed.

Rejection of Claim 59 Under 35 U.S.C. §103(a), based on *Egawa et al.*

Claim 59, which depends from claim 49, adds that forming the gate includes forming a polycrystalline silicon gate having a dopant concentration greater than about 10^{10} atoms/cm^3.

To establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference

[7] *Egawa et al.*, Col. 9, Lines 50-54, referencing the fourth embodiment (emphasis added).

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teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.

To address this ground for rejection Applicant incorporates by reference herein the same comments set forth above for claim 49. Namely, that the reference *Egawa et al.* does not show forming a gate having different conductivity type than a corresponding source and drain region. Accordingly, the reference does not teach or suggest all claim limitations, and a prima facie case of obviousness cannot exist.

In addition or alternatively, any prima facie case of obviousness is rebutted by the teachings of the fourth embodiment of *Egawa et al.*, which teach away from the limitations of base claim 49.

The present claims 49-59 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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